

DATA SHEET

74ALVCH162827

20-bit buffer/line driver, non-inverting,
with 30 Ω termination resistors (3-State)

Product specification

1998 Sep 29

IC24 Data Handbook

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ALVCH162827

FEATURES

- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 12 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Integrated 30 Ω termination resistors

DESCRIPTION

The 74ALVCH162827 high-performance CMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ALVCH162827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NAND Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

The 74ALVCH162827 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

To ensure the high impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f = 2.5\text{ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT | |
|-------------------|---|--|-----------------|------|----|
| t_{PHL}/t_{PLH} | Propagation delay nAn to nYn | $V_{CC} = 2.5\text{V}$, $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$ | 2.9 2.9 | ns | |
| C_I | Input capacitance | | 5 | pF | |
| C_{PD} | Power dissipation capacitance per latch | $V_I = \text{GND to } V_{CC}^1$ | Output enabled | 14 | pF |
| | | | Output disabled | 3 | |

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|---|-----------------------|---------------|------------|
| 56-Pin Plastic TSSOP Type II | $-40^{\circ}\text{C to } +85^{\circ}\text{C}$ | 74ALVCH162827DGG | ACH162827DGG | SOT364-1 |

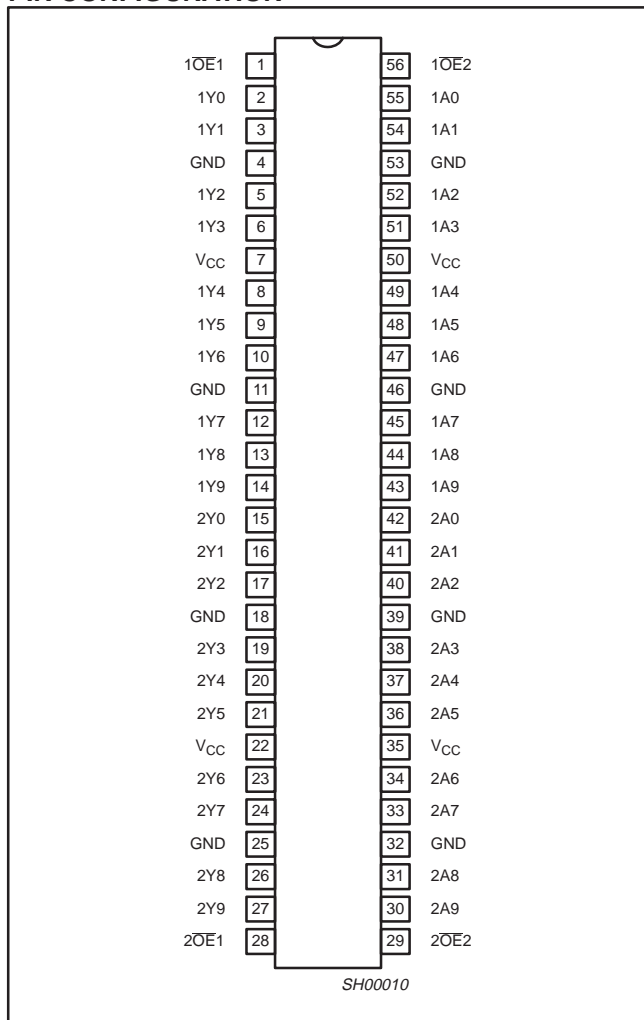
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|---|--|-----------------------------------|
| 55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | 1A0 - 1A9 2A0 - 2A9 | Data inputs |
| 2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27 | 1Y0 - 1Y9 2Y0 - 2Y9 | Data outputs |
| 1, 56, 28, 29 | $1\overline{OE}1$ $1\overline{OE}2$, $2\overline{OE}1$, $2\overline{OE}2$ | Output enable inputs (active-LOW) |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | Ground (0V) |
| 7, 22, 35, 50 | V_{CC} | Positive supply voltage |

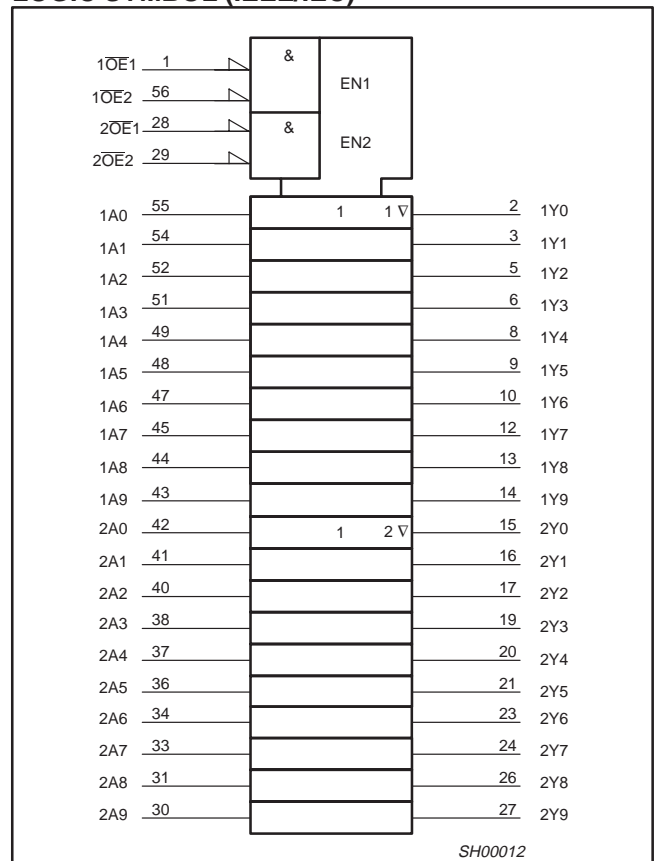
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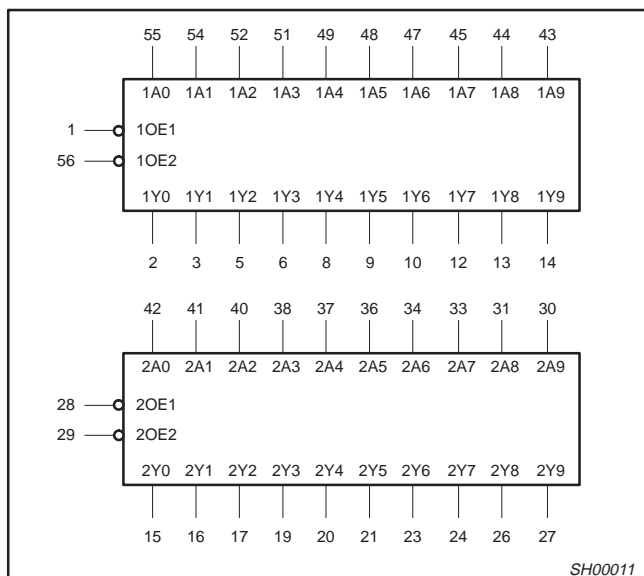
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

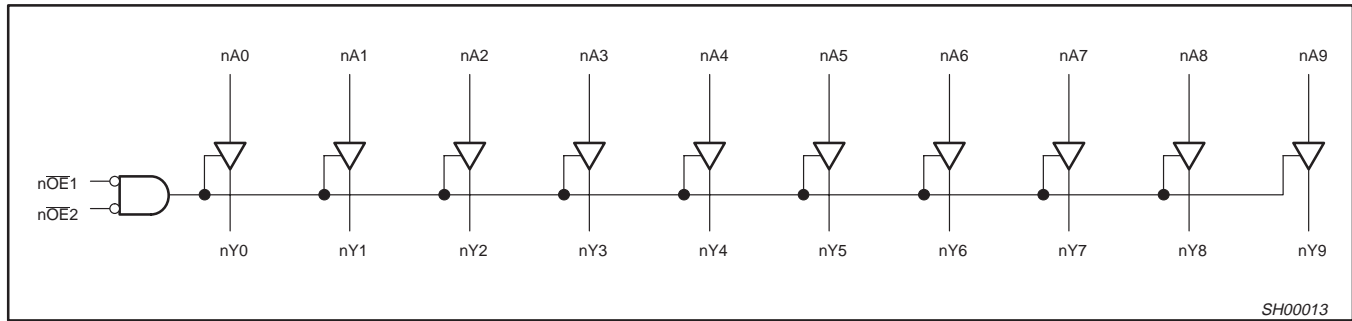
| INPUTS | | | OUTPUT | OPERATING MODE |
|--------|------|-----|--------|----------------|
| nOE1 | nOE2 | nAn | nYn | |
| L | L | L | L | Transparent |
| L | L | H | H | Transparent |
| H | X | X | Z | High impedance |
| X | H | X | Z | High impedance |

- X = Don't care
- Z = High impedance "off" state
- H = High voltage level
- L = Low voltage level

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LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|---------------------------------|---|-------------------------------|-----|-----------------|------|
| V _{CC} | DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load) | | 2.3 | 2.7 | V |
| | DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load) | | 3.0 | 3.6 | |
| V _I | DC Input voltage range | | 0 | V _{CC} | V |
| V _O | DC output voltage range | | 0 | V _{CC} | V |
| T _{amb} | Operating free-air temperature range | | -40 | +85 | °C |
| t _r , t _f | Input rise and fall times | V _{CC} = 2.3 to 3.0V | 0 | 20 | ns/V |
| | | V _{CC} = 3.0 to 3.6V | 0 | 10 | |

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
 Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------------------------|--|--|-------------------------------|------|
| V _{CC} | DC supply voltage | | -0.5 to +4.6 | V |
| I _{IK} | DC input diode current | V _I < 0 | -50 | mA |
| V _I | DC input voltage | Note 1 | -0.5 to +4.6 | V |
| I _{OK} | DC output diode current | V _O > V _{CC} or V _O < 0 | ± 50 | mA |
| V _O | DC output voltage | Note 1 | -0.5 to V _{CC} + 0.5 | V |
| I _O | DC output source or sink current | V _O = 0 to V _{CC} | ± 50 | mA |
| I _{GND} , I _{CC} | DC V _{CC} or GND current | | ± 100 | mA |
| T _{stg} | Storage temperature range | | -65 to +150 | °C |
| P _{TOT} | Power dissipation per package -plastic thin-medium-shrink (TSSOP) | For temperature range: -40 to +125 °C above +55°C derate linearly with 8 mW/K | 600 | mW |

NOTE:

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|-------------------|-------------------------------------|---|-----------------------|------------------------|------|------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V _{IH} | HIGH level Input voltage | V _{CC} = 2.3 to 2.7V | 1.7 | 1.2 | | V |
| | | V _{CC} = 2.7 to 3.6V | 2.0 | 1.5 | | |
| V _{IL} | LOW level Input voltage | V _{CC} = 2.3 to 2.7V | | 1.2 | 0.7 | V |
| | | V _{CC} = 2.7 to 3.6V | | 1.5 | 0.8 | |
| V _{OH} | HIGH level output voltage | V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = -100μA | V _{CC} - 0.2 | V _{CC} | | V |
| | | V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -4mA | V _{CC} - 0.4 | V _{CC} - 0.11 | | |
| | | V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -6mA | V _{CC} - 0.6 | V _{CC} - 0.17 | | |
| | | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -4mA | V _{CC} - 0.5 | V _{CC} - 0.09 | | |
| | | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -8mA | V _{CC} - 0.7 | V _{CC} - 0.19 | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -6mA | V _{CC} - 0.6 | V _{CC} - 0.13 | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA | V _{CC} - 1.0 | V _{CC} - 0.27 | | |
| V _{OL} | LOW level output voltage | V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = 100μA | | GND | 0.20 | V |
| | | V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 4mA | | 0.07 | 0.40 | |
| | | V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 6mA | | 0.11 | 0.55 | |
| | | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 4mA | | 0.06 | 0.40 | |
| | | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 8mA | | 0.13 | 0.60 | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 6mA | | 0.09 | 0.55 | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 12mA | | 0.19 | 0.80 | |
| I _I | Input leakage current | V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND | | 0.1 | 5 | μA |
| I _{OZ} | 3-State output OFF-state current | V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND | | 0.1 | 10 | μA |
| I _{CC} | Quiescent supply current | V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND; I _O = 0 | | 0.2 | 40 | μA |
| ΔI _{CC} | Additional quiescent supply current | V _{CC} = 2.3V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0 | | 150 | 750 | μA |
| I _{BHL} | Bus hold LOW sustaining current | V _{CC} = 2.3V; V _I = 0.7V ² | 45 | - | | μA |
| I _{BHH} | Bus hold HIGH sustaining current | V _{CC} = 2.3V; V _I = 1.7V ² | -45 | | | μA |
| | | V _{CC} = 3.0V; V _I = 2.0V ² | -75 | -175 | | |
| I _{BHLO} | Bus hold LOW overdrive current | V _{CC} = 3.6V ² | 500 | | | μA |
| I _{BHHO} | Bus hold HIGH overdrive current | V _{CC} = 3.6V ² | -500 | | | μA |

NOTES:

- All typical values are at T_{amb} = 25°C.
- Valid for data inputs of bus hold parts.

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

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AC CHARACTERISTICS FOR $V_{CC} = 2.5V \pm 0.2V$

GND = 0V; $t_r = t_f \leq 2.0ns$; $C_L = 30pF$

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|-------------------|--|----------|-------------------------|------------------|-----|------|
| | | | $V_{CC} = 2.5 \pm 0.2V$ | | | |
| | | | MIN | TYP ¹ | MAX | |
| t_{PHL}/t_{PLH} | Propagation delay nAn to nYn | 1, 3 | 1.0 | 2.9 | 4.6 | ns |
| t_{PZH}/t_{PZL} | 3-State output enable time n $\overline{O}En$ to nYn | 2, 3 | 1.4 | 3.9 | 6.4 | ns |
| t_{PHZ}/t_{PLZ} | 3-State output disable time n $\overline{O}En$ to nYn | 2,3 | 1.7 | 2.2 | 5.9 | ns |

NOTE:1. All typical values are at $V_{CC} = 2.5V$ and $T_{amb} = 25^\circ C$.

AC CHARACTERISTICS FOR $V_{CC} = 3.0V \pm 0.3V$

GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | LIMITS | | UNIT |
|-------------------|--|----------|-------------------------|---------------------|-----|------------------|-----|------|
| | | | $V_{CC} = 3.3 \pm 0.3V$ | | | $V_{CC} = 2.7V$ | | |
| | | | MIN | TYP ^{1, 2} | MAX | TYP ¹ | MAX | |
| t_{PHL}/t_{PLH} | Propagation delay nAn to nYn | 1, 3 | 1.5 | 2.9 | 4.2 | 3.1 | 4.7 | ns |
| t_{PZH}/t_{PZL} | 3-State output enable time n $\overline{O}En$ to nYn | 2, 3 | 1.6 | 3.7 | 5.4 | 4.4 | 6.5 | ns |
| t_{PHZ}/t_{PLZ} | 3-State output disable time n $\overline{O}En$ to nYn | 2, 3 | 1.8 | 3.0 | 4.7 | 3.2 | 5.2 | ns |

NOTES:1. All typical values are at $V_{CC} T_{amb} = 25^\circ C$.2. Typical value is measured at $V_{CC} = 3.3V$.

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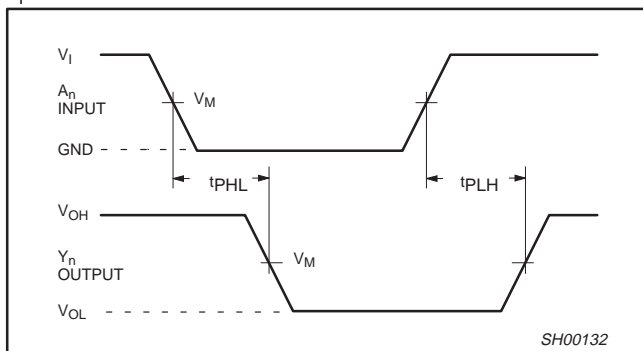
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AC WAVEFORMS FOR $V_{CC} = 2.3V$ TO $2.7V$

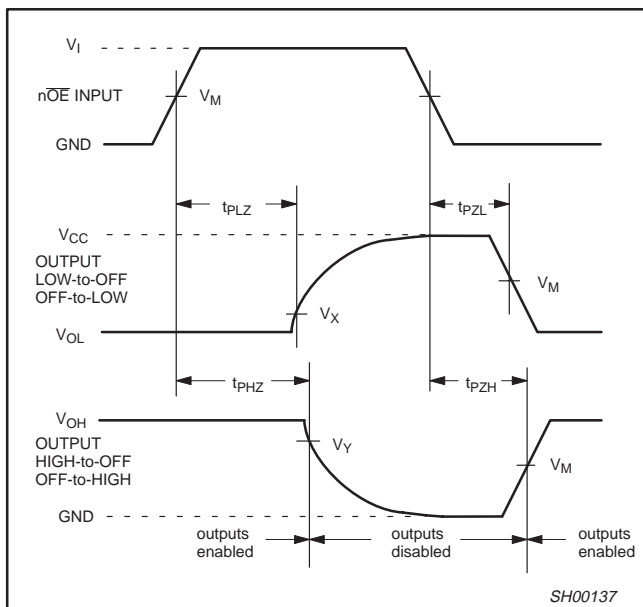
$V_M = 0.5 V_{CC}$
 $V_X = V_{OL} + 0.15V$
 $V_Y = V_{OH} - 0.15V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = V_{CC}$

AC WAVEFORMS FOR $V_{CC} = 3.0V$ TO $3.6V$ AND $V_{CC} = 2.7V$ RANGE

$V_M = 1.5 V$
 $V_X = V_{OL} + 0.3V$
 $V_Y = V_{OH} - 0.3V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = 2.7V$



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM

Test Circuit for switching times

DEFINITIONS
 R_L = Load resistor
 C_L = Load capacitance includes jig and probe capacitance
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

| TEST | S_1 | V_{CC} | V_I |
|-------------------|--------------|----------|----------|
| t_{PLH}/t_{PHL} | Open | < 2.7V | V_{CC} |
| t_{PLZ}/t_{PZL} | $2 * V_{CC}$ | 2.7-3.6V | 2.7V |
| t_{PHZ}/t_{PZH} | GND | | |

SV00906

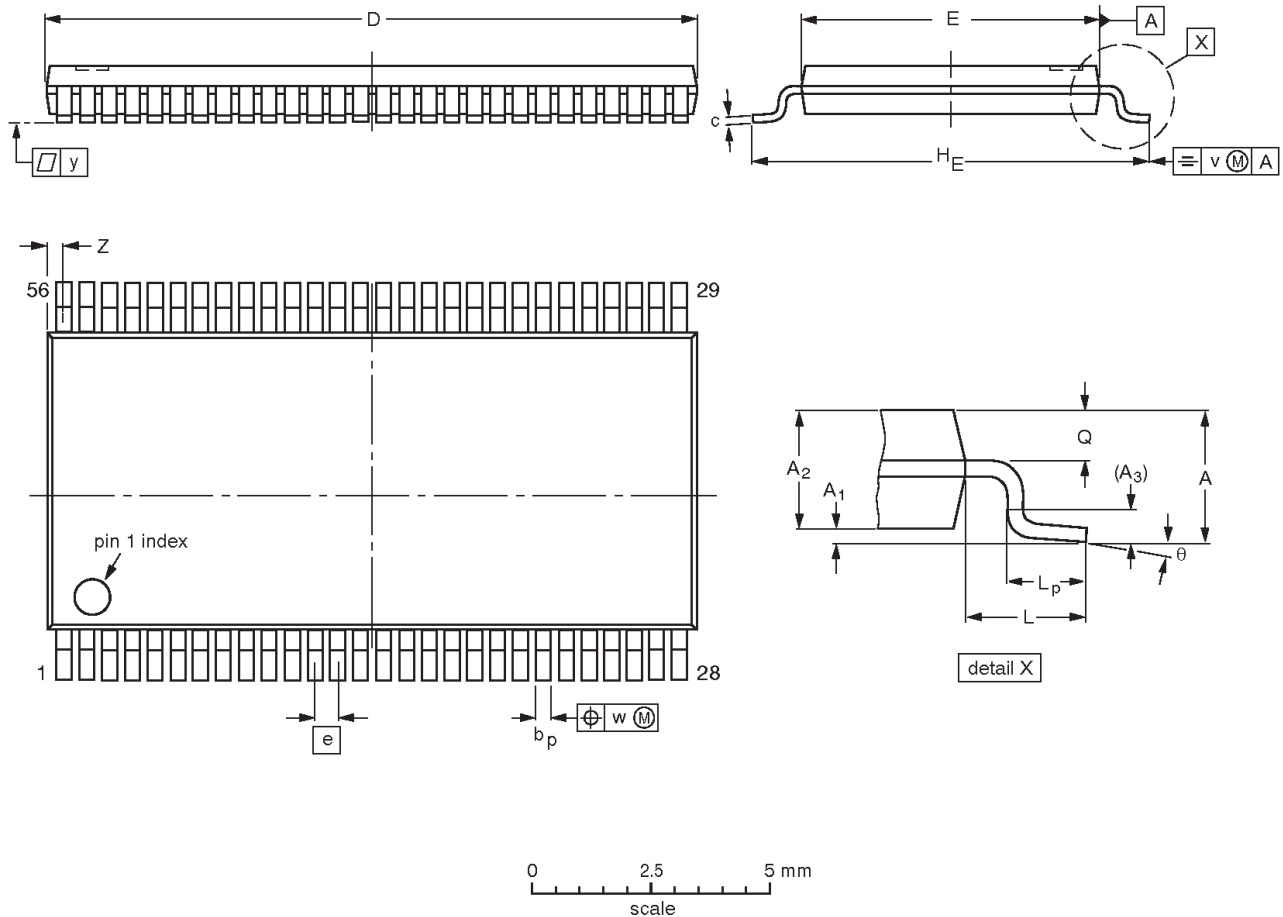
Waveform 3. Load circuitry for switching times

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|-----|----------------|-----|----------------|--------------|------|------|-----|------------|----------|
| mm | 1.2 | 0.15 0.05 | 1.05 0.85 | 0.25 | 0.28 0.17 | 0.2 0.1 | 14.1 13.9 | 6.2 6.0 | 0.5 | 8.3 7.9 | 1.0 | 0.8 0.4 | 0.50 0.35 | 0.25 | 0.08 | 0.1 | 0.5 0.1 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT364-1 | | MO-153EE | | | | 93-02-03 95-02-10 |

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NOTES

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
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